SHARP SERVICE MANUAL

CODE: 00ZPCE220SM/E

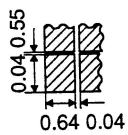
MODEL PC-E220

1. General

The PC-E220 is equipped with the Z80 CPU, 32KB RAM (with memory backup function), and Z80 machine language monitor.

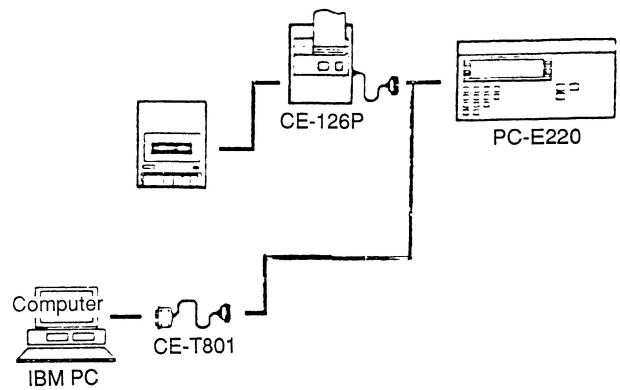
2. Specifications

Model:	PC-E220
Calculation digits:	10 digits + 2 digits
Calculation system:	Formula order (Priority judgment function)
Program language:	BASIC, ASSEMBLER
CPU:	CMOS Z80A (8 bit)
RAM:	32KB (system area approx. 2.1KB, program/data area 30435B, data area 208B), with RAM file function.
Stack:	Subroutine stack: 10 buffers Function stack: 16 buffers FOR-NEXT stack: 5 buffers Data stack: 8 buffers
Editing functions:	Cursor shift (right/left) (▶ , ◀), insertion (INS), delete (DEL) List up, list down (↑, ↓), back space (BS), text editor, Z80 machine language monitor
Interface:	11 pin interface (for cassette interface, printer, SIO device)
Display:	5 x 7 dot matrix LCD (24 digits x 4 lines)

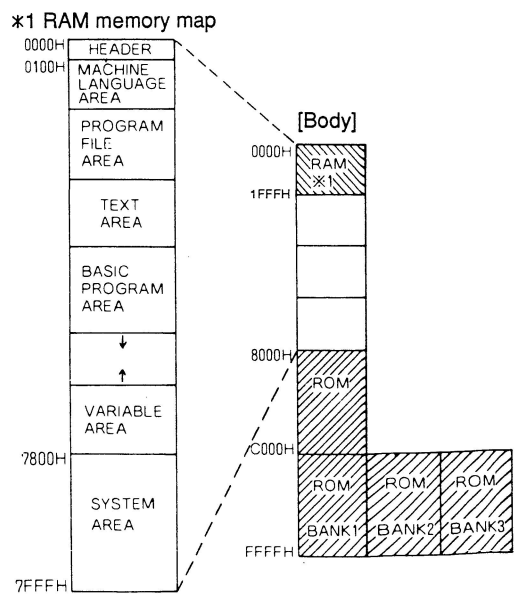


Memory protection:	Battery backup
Operating temperature:	0°C ~ 40°C (32° ~ 104°F)
Power supply:	For computer operation: 6.0 Vdc Type-AA dry cell battery (R06) x 4 For memory backup: 3.0 Vdc Lithium battery (CR2032) x 1
Battery lifetime:	Approximately 80 hours of continuous operation under normal conditions (based on 10 minutes of operation or program execution and 50 minutes of display per hour at a temperature of 20°C/68°F). Note: When the computer is used for serial communications through the optional CE-T801 Data Transfer Cable, the number of hours the unit can be operated continuously will drop to approx. 48 hours (when used for 2 min. of communications, 8 min. of calculation or program execution, and 50 min. of display per hour at an ambinet temperature of 20°C/68°F). The operating time may vary slightly depending on usage and the brand of battery used.
Power consumption:	0.37W
External dimensions:	215mm(W) x 100mm (D) x 18mm (H) 8 15/32" (W) x 3 15/16" (D) x 23/32" (H)
Weight:	280g (0.62 lb.) (Including the battery, without hard case)
Accessories:	Hard cover, four AA batteries, one lithium battery, and Operation manual

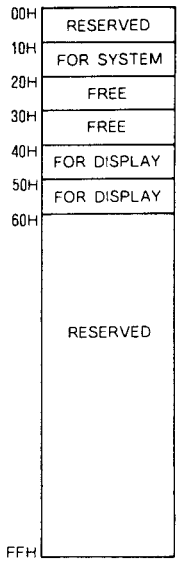
3. System configuration



4. Memory map



5. I/O map



Name	Function	Pin function	Bit map	READ	WRITE	ADDRESS
IA1-IA8	KEY common input	IN (Including a pull-down resistor)	MSB 8 7 6 5 4 3 2 1 LSB	○	×	10H
KO1-KO8	KEY strobe	OUT (Pch open drain)	MSB 8 7 6 5 4 3 2 KO 1 LSB	×	○	11H
KO9, KO10	KEY strobe	OUT (Pch open drain)	MSB KO 10 KO 9 LSB	×	○	12H
SFTIN	SHIFT key input	IN (Including a pull down resistor)	MSB SFT LSB	○	×	13H
Timer	1S signal is set about every 0.6 sec.	—	MSB 1S LSB (Note) After judgement of 1S signal, procedure 01H → OUT (14H) must be performed to reset 1S signal latch.	○	○	14H
XIN control	Controls on/off of XIN input.	IN	MSB XIN ON/OFF LSB 0: XIN input inhibit 1: XIN input enable	○	○	15H
Maskable interrupt factor	Indicates interrupt generating factor with the interrupt mask ON.	—	MSB $\overline{INT1}$ 1S KON IA LSB Conditions for becoming "1": When IA-IA key input signal is supplied. When KON-KON key input is supplied. 1S-0.6 sec timer signal is supplied. A low pulse is supplied to $\overline{INT1}$-$\overline{INT1}$ input pin. To reset each factor, write "1." With 0FH → OUT (16H), all factors become 0.	○	○	16H

<table>
<tr><th>Name</th><th>Function</th><th>Pin function</th><th>Bit map</th><th>READ</th><th>WRITE</th><th>ADDRESS</th></tr>
<tr><td>Interrupt mask</td><td>Performs interrupt enable/inhibit of each interrupt factor.</td><td>—</td><td>MSB LSB
<table><tr><td></td><td></td><td></td><td></td><td>INT1</td><td>1S</td><td>KON</td><td>IA</td></tr></table>0: Interruption inhibit
1" Interruption enable</td><td>○</td><td>○</td><td>17H</td></tr>
<tr><td>FO1, FO2, XOUT</td><td>11 pin interface output control port</td><td>OUT FO1, FO2
(Pch open drain)</td><td>MSB LSB
<table><tr><td>X
OUT</td><td></td><td></td><td></td><td></td><td></td><td>FO
2</td><td>FO
1</td></tr></table>0: Low output
1: High output</td><td>○</td><td>○</td><td>18H</td></tr>
<tr><td>BNK0
BNK1
BNK2</td><td>When making access to C000H ~ FFFFH
<table><tr><th>Output pin</th><th>Input pin</th></tr><tr><td>BNK0</td><td>BK0</td></tr><tr><td>BNK1</td><td>BK1</td></tr></table>$\overline{\text{CEROM1}}$ signal is supplied (Active low)

When making access to 8000H ~ BFFFH
<table><tr><th>Output pin</th><th>Input pin</th></tr><tr><td>BNK0</td><td>BK'0</td></tr><tr><td>BNK1</td><td>BK'1</td></tr><tr><td>BNK2</td><td>BK'2</td></tr></table>$\overline{\text{CEROM2}}$ signal is supplied. (Active Low)</td><td>OUT</td><td>MSB LSB
<table><tr><td></td><td>BK'
2</td><td>BK'
1</td><td>BK'
0</td><td></td><td></td><td>BK
1</td><td>BK
0</td></tr></table>• Supplied to BNK0 and BNK1 pins when making access to BK0, BK1 system ROM bank port C000H ~ FFFH.
<table><tr><th>BK1</th><th>BK0</th><th>C000H ~ FFFFH bank specification</th></tr><tr><td>0</td><td>0</td><td>—</td></tr><tr><td>0</td><td>1</td><td>BANK1</td></tr><tr><td>1</td><td>0</td><td>BANK2</td></tr><tr><td>1</td><td>1</td><td>BANK3</td></tr></table>• Supplied to BNK2, BNK1, and BNK0 pins when making access to BK'2=BK'0 (expansion back port) 8000H ~ BFFFH.
<table><tr><th>BK' 2</th><th>BK' 1</th><th>BK' 0</th><th>8000H ~ BFFFH bank specification</th></tr><tr><td>1</td><td>0</td><td>0</td><td>EXBANK0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>EXBANK1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>EXBANK2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>EXBANK3</td></tr></table>By driving BK'2 to "1," the system ROM 8000H ~ BFFFH is separated.</td><td>○</td><td>○</td><td>19H</td></tr>
<tr><td>CERAM1
CERAM2</td><td>Chip enable signal supplied when making access to 0000H ~ 7FFFH (Active high)</td><td>OUT</td><td>MSB LSB
<table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>SLOT</td><td></td></tr></table>SLOT=0: CERAM1 is effective.
SLOT=1: CERAM2 is effective.</td><td>○</td><td>○</td><td>1BH</td></tr>
<tr><td>IORESET</td><td>Expansion peripheral RESET</td><td>OUT</td><td>MSB LSB
<table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td>IOR</td><td>X</td></tr></table>"0" must be written into this bit.
<table><tr><th>IOR</th><th>IORESET</th></tr><tr><td>0</td><td>Low</td></tr><tr><td>1</td><td>High</td></tr></table>• When the set power source is turned on and when the reset key is pressed, a high pulse is supplied to IORESET.</td><td>×</td><td>○</td><td>1CH</td></tr>
<tr><td>IB1, IB2
XIN

KON</td><td>11 pin interface input port (IB1 and IB2 are equipped with pull down resistor.)

ON Break key input</td><td>IN</td><td>MSB LSB
<table><tr><td>KON</td><td></td><td></td><td></td><td></td><td>XIN</td><td>IB
2</td><td>IB
1</td></tr></table>XIN input is enable when XIN control port is at "1."</td><td>○</td><td>×</td><td>1FH</td></tr>
</table>

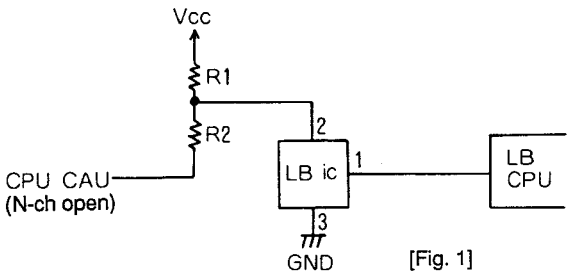
6. LSI descriptions

CPU (LZ8413M) pin signal descriptions

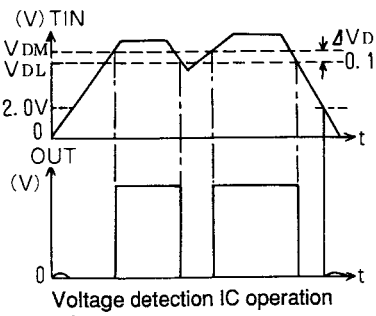
Pin No.	I/O	Signal name	Description
1	O	KO2	Key strobe
2	O	KO3	Key strobe
3	O	KO4	Key strobe
4	O	KO5	Key strobe
5	O	KO6	Key strobe
6	O	KO7	Key strobe
7	O	KO8	Key strobe
8	O	KO9	Key strobe
9	O	KO10	Key strobe
10	I	IA1	Key input
11	I	IA2	Key input
12	I	IA3	Key input
13	I	IA4	Key input
14	I	IA5	Key input
15	I	IA6	Key input
16	I	IA7	Key input
17	I	IA8	Key input
18	I/O	$\overline{\text{MREQ}}$	Z80CPU memory request signal
19	I/O	$\overline{\text{IORQ}}$	Z80CPU I/O request signal
20	I	$\overline{\text{BUSRQ}}$	Z80CPU bus request signal
21	O	IORESET	Expansion peripheral reset output (Active high) (40 pin expansion bus output)
22	I	$\overline{\text{WAIT}}$	Z80CPU wait input
23	I	$\overline{\text{INT1}}$	Z80CPU maskable interrupt request
24	I/O	$\overline{\text{WR}}$	Z80CPU memory write signal
25	I/O	$\overline{\text{RD}}$	Z80CPU memory read signal
26	I/O	BNK3	Bank select address (When resetting, domestic/foreign select signal)
27	I/O	BNK2	Bank select address
28	O	BNK1	Bank select address
29	O	BNK0	Bank select address
30	O	$\overline{\text{CEROM2}}$	Expansion memory chip enable signal (Outputted to 40 pin expansion bus)
31	O	$\overline{\text{CEROM1}}$	Built-in system ROM chip enable signal
32	—	GND	Reference voltage
33	O	CERAM2	Expansion memory chip enable signal (Outputs to 40 pin expansion bus.)
34	O	CERAM1	Built-in RAM chip enable signal
35	I	IB2	11 pin ACK
36	I	IB1	11 pin DIN
37	O	XOUT	Cassette signal output
38	I	XIN	Cassette signal input
39	O	FO2	11 pin DOUT
40	O	FO1	11 pin BUSY
41	I/O	D7	Data bus
42	I/O	D6	Data bus
43	I/O	D5	Data bus
44	I/O	D4	Data bus
45	I/O	D3	Data bus
46	I/O	D2	Data bus
47	I/O	D1	Data bus
48	I/O	D0	Data bus
49	I/O	A15	Address bus
50	I/O	A14	Address bus
51	O	A13	Address bus
52	O	A12	Address bus
53	O	A11	Address bus
54	I/O	A10	Address bus
55	O	A9	Address bus
56	O	A8	Address bus
57	I/O	A7	Address bus
58	I/O	A6	Address bus
59	I/O	A5	Address bus
60	I/O	A4	Address bus
61	I/O	A3	Address bus
62	I/O	A2	Address bus
63	I/O	A1	Address bus
64	I/O	A0	Address bus
65	I	$\overline{\text{RESET}}$	Reset input (Reset at LOW)
66	O	E	Liquid crystal driver enable signal
67	I	M	Timer clock input
68	I	$\overline{\text{LB}}$	Low battery detection pin. Low when low battery.
69	O	CAU	Low battery symbol lighting voltage detection pin. (After turning on the symbol, high impedance.)
70	I	XTAL1	Oscillation circuit input
71	O	XTAL2	Oscillation circuit output
72	—	GND	Power source ⊖
73	O	CLKOUT	Oscillation clock output
74	—	VCC	Power source ⊕
75	O	VCNT	Liquid crystal power ON/OFF SW signal
76	O	BZ	BUZZER
77	I/O	$\overline{\text{M1}}$	Z80CPU machine cycle
78	I	KON	CN KEY input
79	I	SFTIN	SHIFT KEY input
80	O	KO1	Key strobe

7. Low battery detection circuit

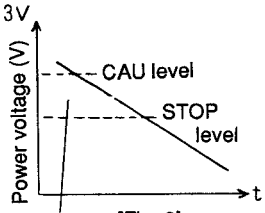
This unit is equipped with the low battery detection circuit. Its operations are described below. (The parts location numbers are different from the actual ones.)
As shown below, when the input voltage VIN exceeds detection voltage VD, the output becomes HIGH from LOW. When VIN falls below DIN, the output becomes LOW.
The LBIC (MN1280) detects the CAU level and the STOP level with one IC.
To achieve this, the input voltage applied to the input pin (2 pin) is divided with R1 and R2, and R2 is turned on/off by the CAU signal.
As shown in Fig. 3, when the power voltage falls below the CAU level, the BATT symbol lights up. When it falls further below the STOP level, it is turned off.
To detect the CAU level, the CPU CAU pin is turned on (at low level) and the LB pin of the CPU is checked. (If the LBC pin is low, the symbol lights up.)
After detecting the CAU level, the CAU pin is turned off (at HIGH.) (When the CAU pin is turned off, the resistor division is not performed and the potential at BIC 2 pin rises to drive the output to HIGH.) Then the CPU LB pin is checked again to detect the STOP level.
After detecting the STOP level, the ON/BRK key and the RESET switch do not work.



[Fig. 1]



Voltage detection IC operation
[Fig. 2]

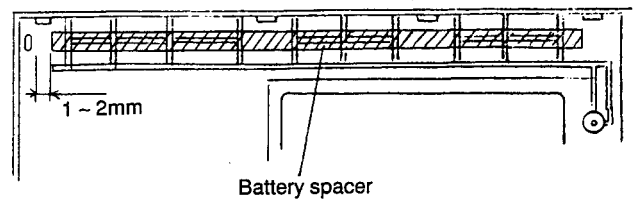


Symbol lights up.
[Fig. 3]

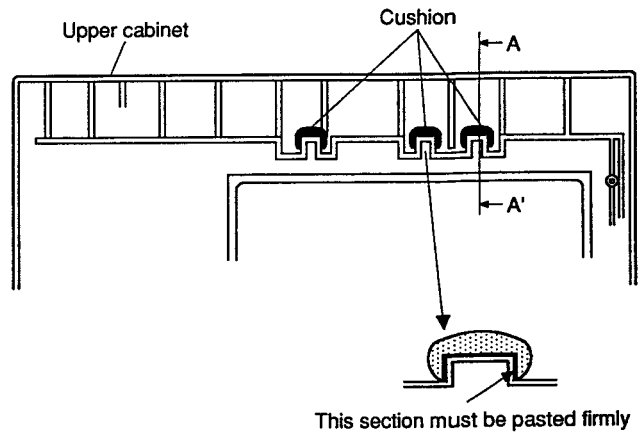
8. Note for servicing

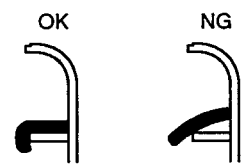
1. Cabinet upper unit

◎ Battery spacer attachment



2. Battery holder cushion attachment

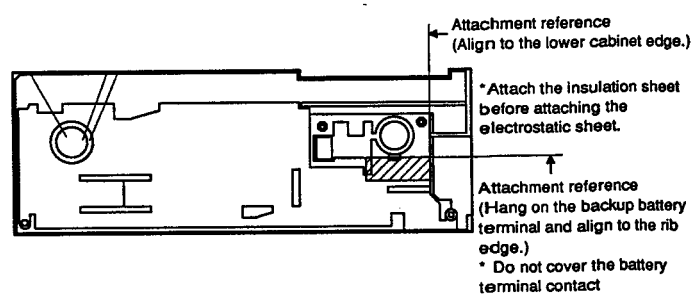




A-A' cross section

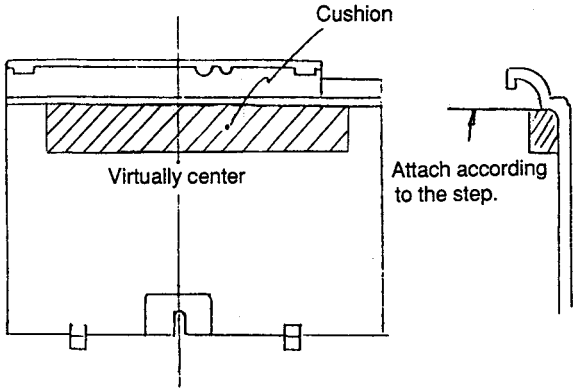
* The cushion must be attached securely. After the cushion glue is dried, it cannot be reattached.
This part must be attached.

3. Coin screw insulation sheet attachment

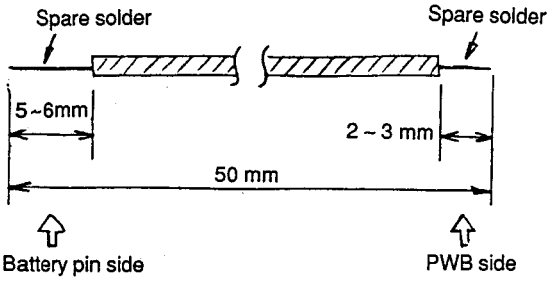


4. Battery cover

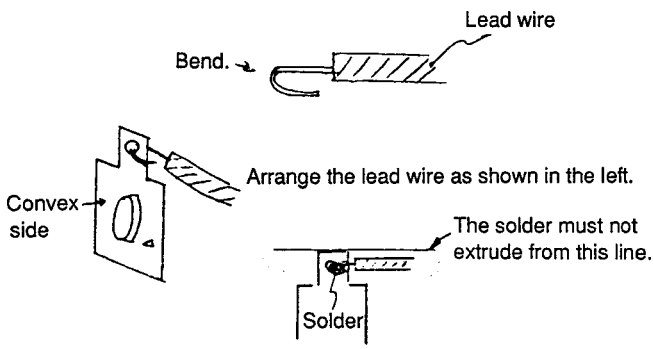
◎ Cushion attachment



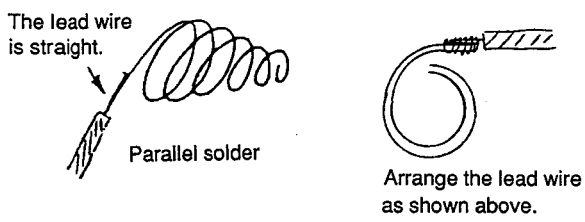
5. Battery pin



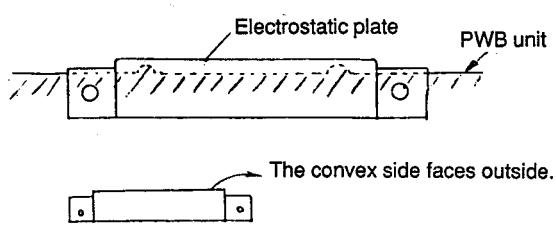
◎ ⊕ pin soldering



◎ ⊖ pin soldering

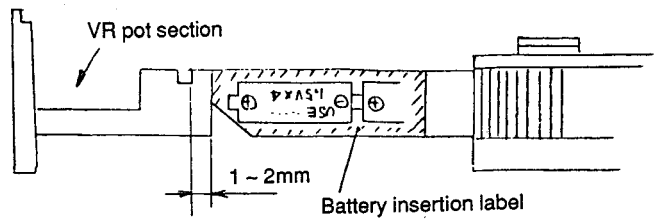


6. Electrostatic plate

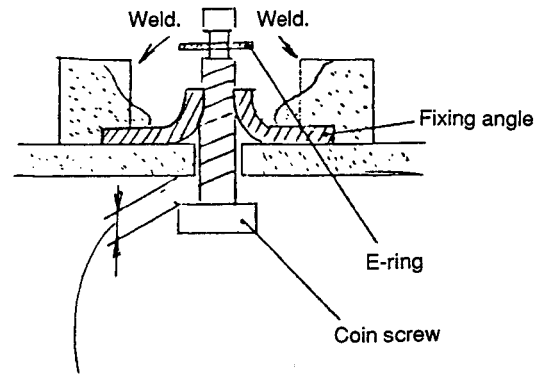


7. Cabinet bottom

◎ Battery insertion label attachment



◎ Coin screw section



When attaching the cabinet bottom unit to the cabinet upper unit, allow a clearance of 1 ~ 2mm between them. (Do not fix the coin screw tightly.)

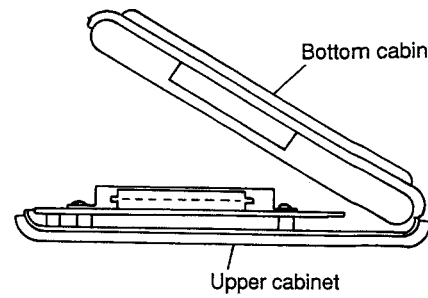
8. Battery current consumption

OFF	25.5μA or less
Displaying	6.93mA or less
Calculating	26.5mA or less

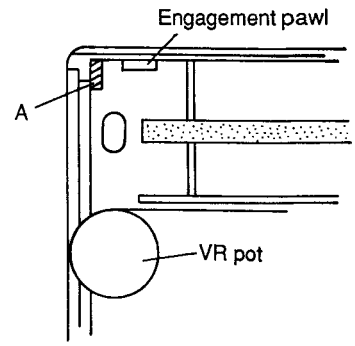
The values in the above table are those in normal temperature of 20°C. They will depend on the surrounding conditions.

9. Upper and lower cabinets engagement

① Fit the upper cabinet pawls with lower cabinet pawls. (4 positions)

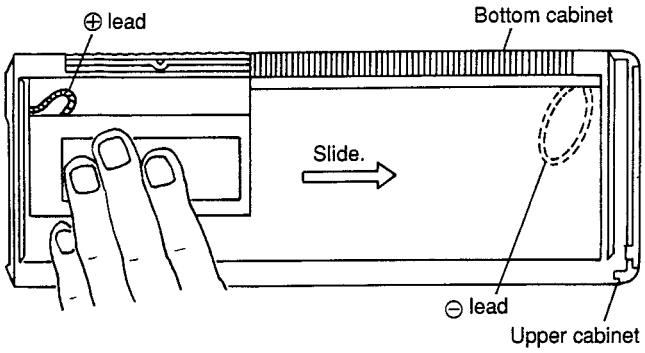


② With the pawls engaged (at 4 positions), slide the bottom cabinet to the VR pot side.



The bottom cabinet must be shifted until it makes contact with the upper cabinet rib (A).

③ Under the state of ②, lightly press the VR pot in the bottom cabinet. (At that time, the lead wires of ⊕ pin and ⊖ pin must be as shown below:

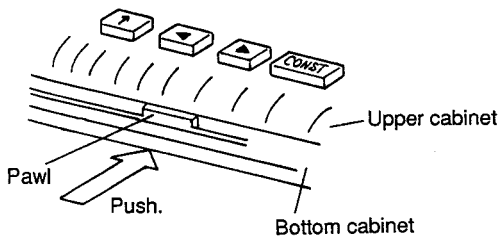


④ Slightly pressing with fingers, slide the bottom cabinet to the right as shown above.

- At that time, check that the VR pot is in the bottom cabinet hole.
- Be careful not to make contact between the VR pot and the bottom cabinet as far as possible to prevent scratching.

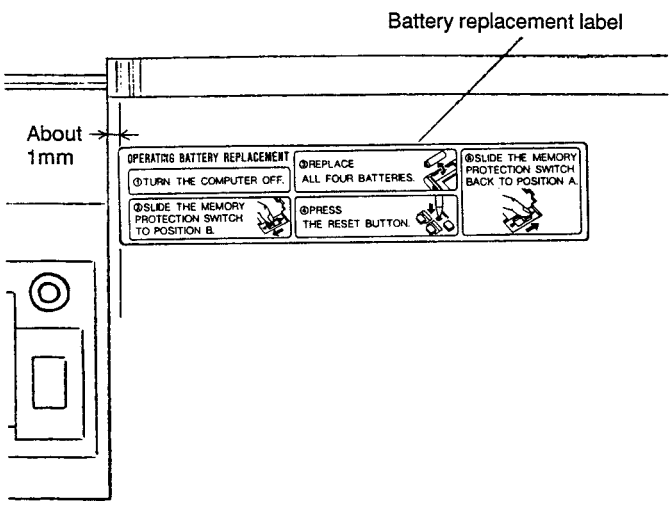
⑤ Extend the 11 pin side of the bottom cabinet and attach the bottom cabinet.

⑥ Engage a pawl in your side with its corresponding hole.



Push the pawl section of the bottom cabinet to insert.

9. Battery replacement caution label attachment



10. Diag.

Starting procedure

Turn on the power switch. While pressing the [SHIFT] key, press the [,] key and press the reset switch.

Menu screen

ROM version name

```
** PC-E220 V.0 CHECK **
1: TOTAL      2: B/U. KEY
3: SHOCK      4: AGIN
5: KEY
```

Note: Only 1 and 2 are used for servicing.

1. Diag. check

Press [1] key. (Total)

A beep sounds once.

RAM check

ROM check

11 pin check (Refer to 2.)

[C] [0] [↵]

RAM backup data write

Display check

Press the return key.

Display reversion check

Press the return key.

Press the RESET key.

OFF (Do not press [Y] key.)

Remove the battery according to the battery replacement procedure.

Insert the battery again.

Put the machine into the diag mode.

Press [2] key. (B/U key)

Press the return key.

```
RAM CHECKING
RAM CHECK OK
ROM CHECKING
ROM CHECK OK
```

```
I/O CHECKING
I/O ERROR

B/U DATA WRITING
```

```
BUSY カナ 2ndF G CONST E
RUN CASL STAT
```

```
CAPS 小 DE RAD M BATT
PRO TEXT PRINT
```

```
ON
```

```
RAM B/U DATA CHECKING
B/U DATA CHECK OK
```

```
ON
```

PC-E220

Key check
(Press the key which is displayed in the right under section of the screen.)

Press the RESET key.

Press [Y] key.

End (Off)

*********	*
*********	*
*********	*
*********	SFT

Press the Shift key.

KEY CHECK O.K.

* • In case of an error, press [C], [O], and [J] then go to the next step.
  • The data registered in the body are erased.

2. Pocket computer body 11 pin check

1) Tool UKOGC3020CSZZ, price rank "BC"
2) Check program (Input into the pocket computer.)

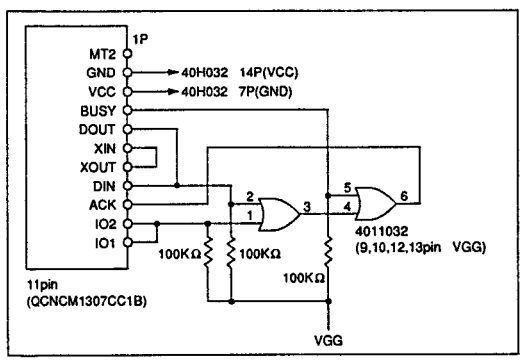
```
10 : FOR I = Ø TO 7
20 : OUT I
30 : PRINT I ; "=>" ; "␣" ; INP ; "␣" ;
40 : NEXT
```

3) Connect the tool shown in 1) with 11 pin of the pocket computer.
4) Execute the check program shown in 2)
5) If the result is as shown below, it is O.K.

Ø. = > Ø.	1. = > 4.	2. = > 3.
3. = > 7.	4. = > 1.	5. = > 5.
6. = > 3.	7. = > 7.	

OUT INP OUT INP OUT INP

6) Tool circuit diagram



7) Check code list

		0	1	2	3	4	5	6	7	← OUT
OUT	H BUSY	0	0	0	0	1	1	1	1	
	M DOUT	0	0	1	1	0	0	1	1	
	L XOUT	0	1	0	1	0	1	0	1	
INP	H XIN	0	1	0	1	0	1	0	1	
	M DIN	0	0	1	1	0	0	1	1	
	L ACK	0	0	1	1	1	1	1	1	
		0	4	3	7	1	5	3	7	←IN

8) If the pocket computer check is O.K., go to the nest step (CE-T801 check).

2. CE-T801 check

1. Operation check

1) Check program (Input this program into the pocket computer.)

```
100 : CLS : WAIT : E = Ø
200 : FOR I = Ø TO 7
300 : OUT I : READ A
400 : IFA < > INP PRINT "ERROR" ; I ; "=>" ;
      INP ; "(" ; A ; ")" : E = I
500 : NEXT
600 : IF E = Ø PRINT "OK!"
700 : DATA 0, 0, 0, 4, 0, 0, 1, 5
800 : OUT Ø
900 : END
```

2) Short the CE-T801 25 pin connector by using the D-SUB male connector as shown below:

2. TXD(XIN) — Short — 3. RXD(XOUT)

4. RS (ACK) — Short — 5. CS (BUSY)

3) Connect the connector shorted by the CE-T801 with the pocket computer.
4) Execute the check program shown in 1).
5) If O.K. sign is displayed, the operation check is completed.
6) In case of an error

Display example:
ERROR 3.= > Ø. (4.)

Normal code
Error code
Check number

Check code table

No.	Output			Input			Code
	BUSY	DOUT	XOUT	XIN	DIN	ACK	
0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
2	0	1	0	0	0	0	0
3	0	1	1	1	0	0	4
4	1	0	0	0	0	0	0
5	1	0	1	0	0	0	0
6	1	1	0	0	0	1	1
7	1	1	1	1	0	1	5

3. Output voltage check

1) Check program (Input this program into the pocket computer.)

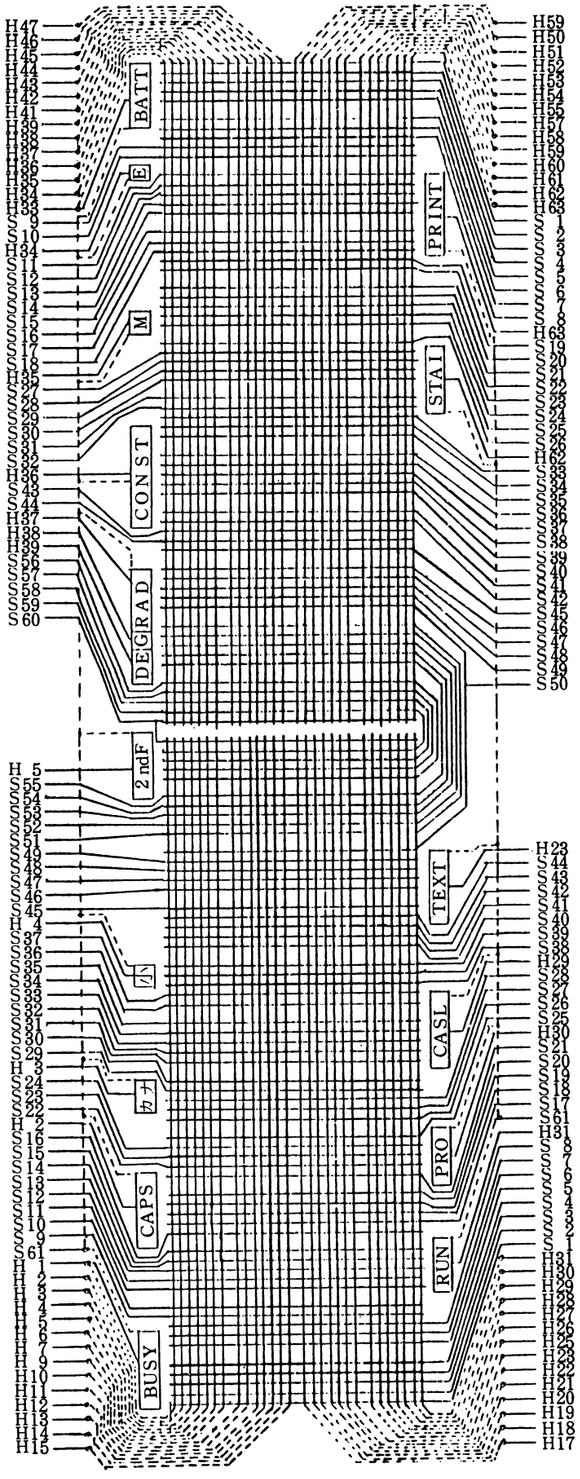
```
1000 : CLS : WAIT
1100 : OUT 3
1200 : PRINT "CHECK 3PIN : HIGH, 5PIN : LOW"
1300 : OUT 6
1400 : PRINT "CHECK 3PIN : LOW, 5PIN : HIGH "
1500 : OUT 0
1600 : END
```

2) Connect the CE-T801 with the pocket computer.
3) Execute the program shown in 1).
4) Check contents

	Display	3 pin (RXD)	5 pin (CS)
1.	CHECK 3PIN : HIGH : 5PIN : LOW	+3V ~ +15V	−3V ~ −15V
2.	CHECK 3PIN : LOW, 5PIN : HIGH	−3V ~ −15V	+3V ~ +15V

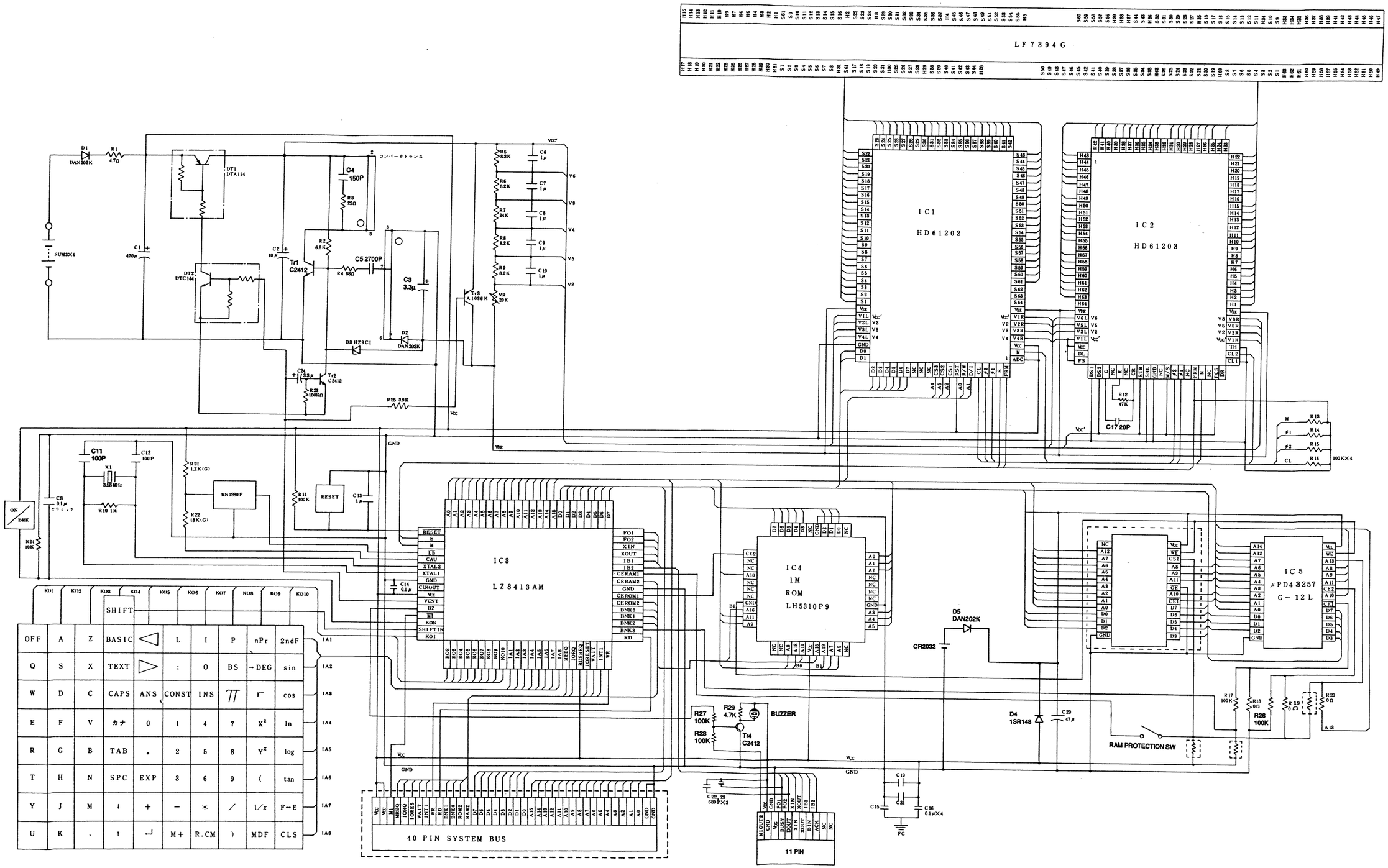
- With the above display, check the voltage at 3 pin and 5 pin with a voltmeter. (7 pin VGG, 3 pin and 5 pin voltages)
- After checking of 1), press the return key and execute the checking of 2).
- If the output voltage is 7 ~ 8V, it is O.K.

11. LCD connecting diagram

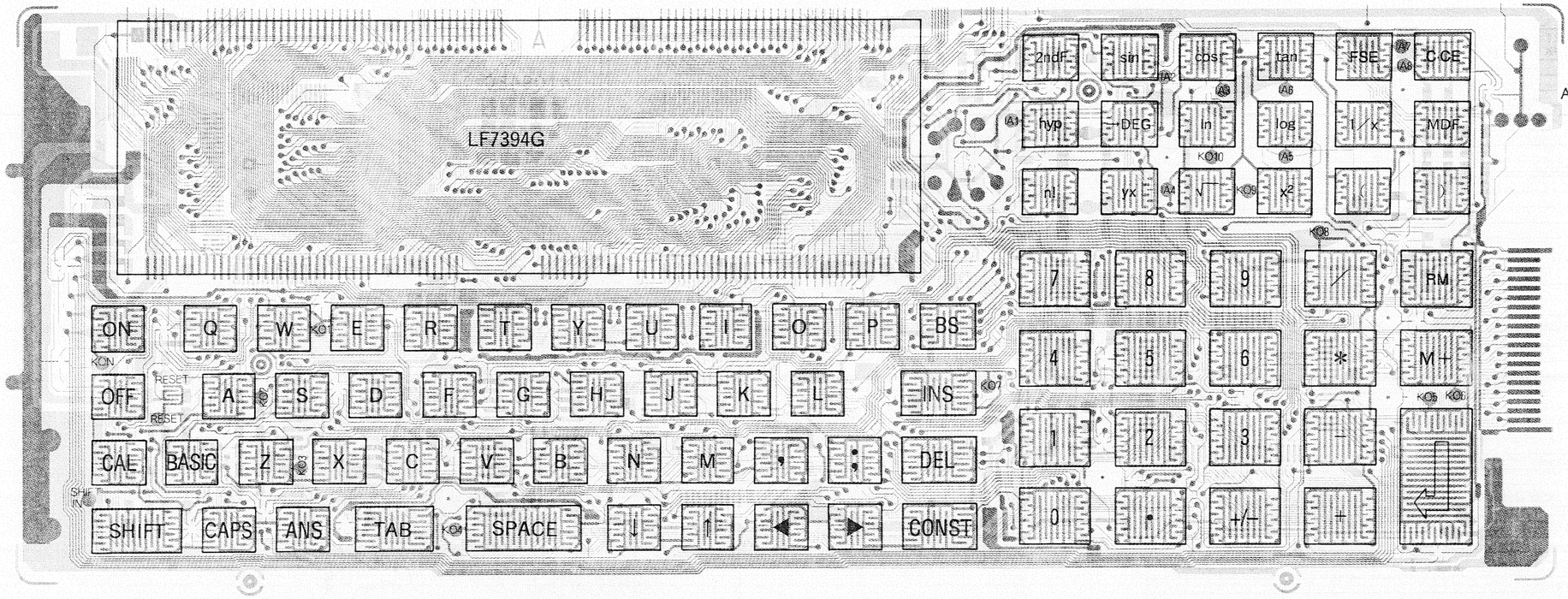


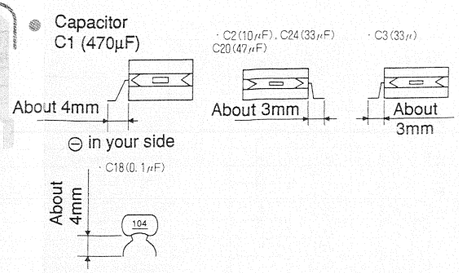
12. Circuit diagram

Note 1: For the dotted line section, refer to the pattern only.
Note 2: C is 25WV 0.1μF capacitor, unless otherwise specified.
Note 3: R is 1/8W J rank resistor unless otherwise specified.



13. Part signal arrangement





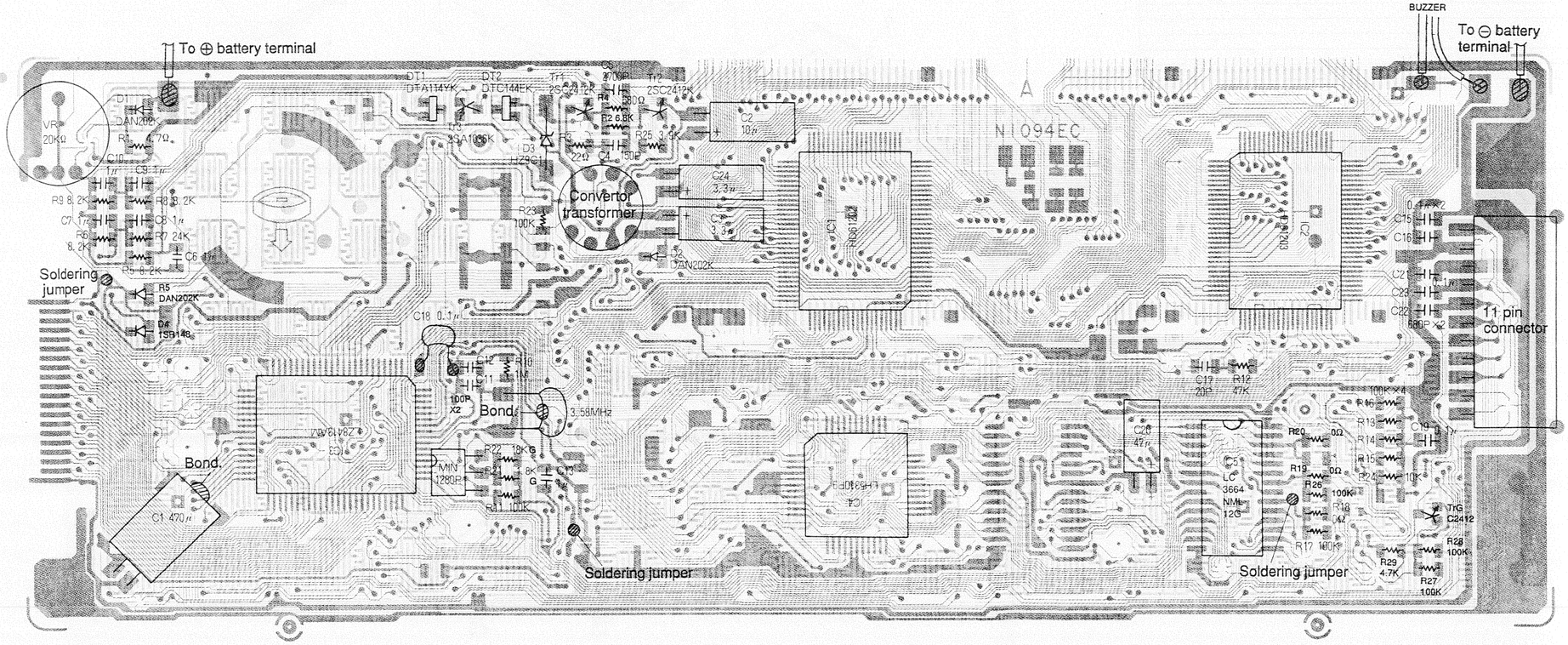
Note for rear attachment parts attachment

- C1 (470µF)
  Solder and bond C1 to the PWB as shown in the parts arrangement pattern. C1 must be in close contact with the PWB.
- MN1280P

When the MN1280 is attached, its molded section comes on the LZ8413M lead.
Solder it so that its height is max. 5mm as shown above.

For the other parts also, solder so that they make close contact with the PWB.

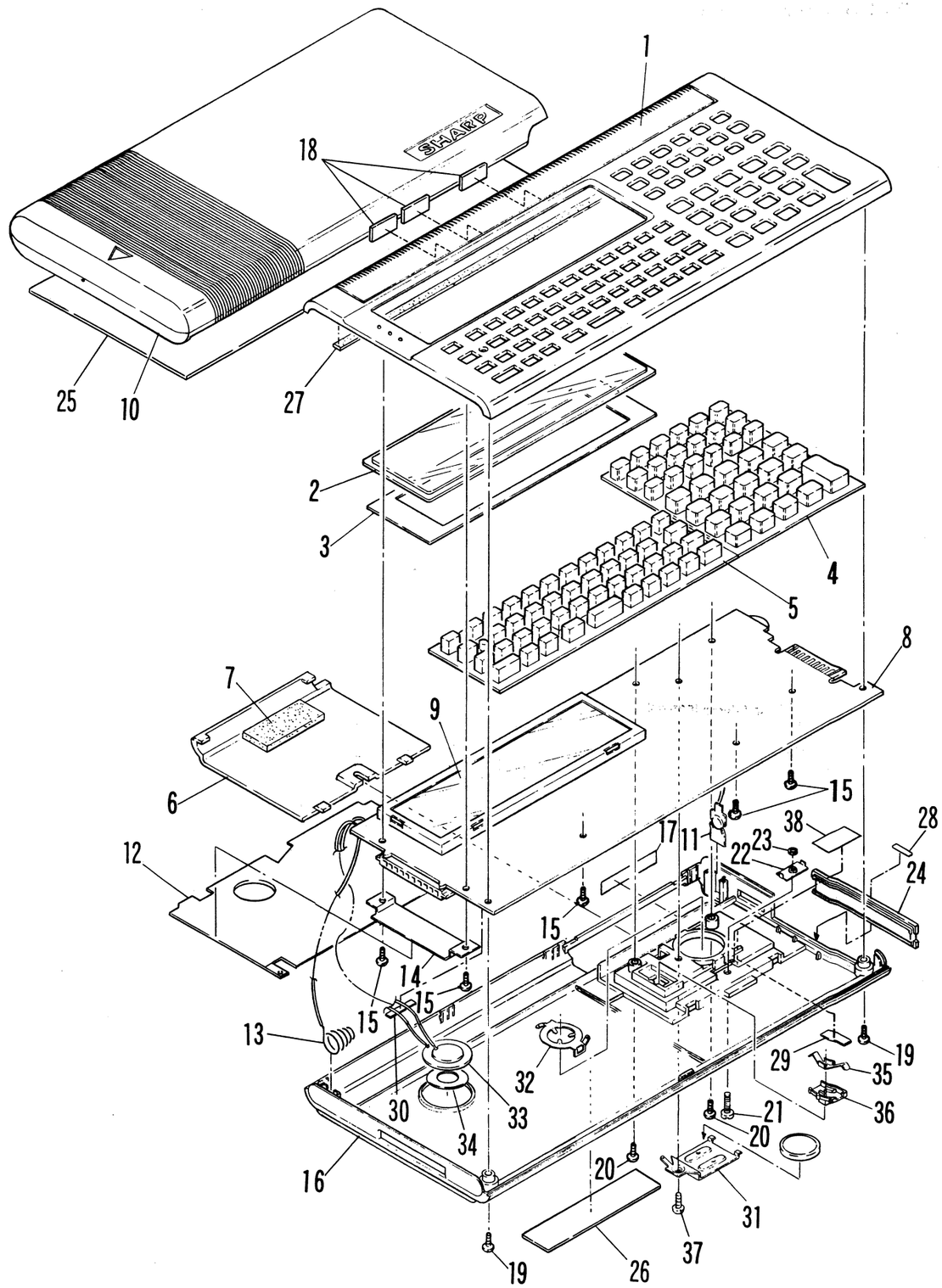
- Jumper wire
  Treat the jumper wires so that they are not entangled.



11. Parts list & guide

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GCABB1041EC09	AL	N	D	Top cabinet
2	PFiLW1010ECZZ	AD		D	Acryl filter
3	PSLDP1024ECSB	AC	N	C	Display mask
4	PGUMM1024EC01	AM	N	B	Key rubber A
5	PGUMM1026EC01	AL	N	B	Key rubber B
6	GFTAB1014EC01	AB	N	D	Battery lid
7	PCUSS1018ECZZ	AA	N	C	Cushion for battery fixing
8	DUNTK1461ECZZ	BS	N	E	Main PWB unit
9	DUNT-1434ECZZ	AV	N	E	LCD unit
10	GCASP1004EC03	AF	N	D	Hard case
11	QTANZ1124CCZZ	AA		C	Battery terminal ⊕
12	PTPEH1050ECZZ	AQ	N	C	Shield tape
13	QTANZ1022ECZZ	AA	N	C	Battery terminal ⊖
14	PSLDC1025ECZZ	AB	N	C	Electrostatic plate
15	LX-BZ1147CCZZ	AA		C	Screw (2×4.5)
16	GCABA1040EC07	AG	N	D	Bottom cabinet
17	TLABZ1273ECZZ	AA	N	D	Battery installation label
18	PCUSS1021ECZZ	AA	N	C	Battery fixing cushion
19	XUBSF20P10000	AA		C	Screw (2×10)
20	XUBSD20P10000	AA		C	Screw (2×10)
21	LX-BZ1021ECZZ	AB	N	C	Screw (Coin screw)
22	LANGT1216CC01	AB		C	Fixing angle
23	XRESP12-0300T	AA	N	C	E type ring
24	GFTAA1020ECZZ	AB	N	D	Connector lid
25	TLABZ1288ECZZ	AD	N	D	Operation label
26	TLABZ1286ECZZ	AC	N	C	Battery replacement label
27	PSPAZ1010ECZZ	AB	N	C	Battery spacer
28	PTPEH1437CCZZ	AA		C	Duplex adhesive tape for crystal
29	TLABH1289ECZZ	AB	N	C	Battery indication label
30	PTPEH1045ECZZ	AA	N	C	Fixing tape (for lead wire)
31	QTANZ1504CCZZ	AB		C	Battery terminal B
32	QTANZ1503CCZZ	AB		C	Battery terminal A
33	RALMB1030CC01	AD		B	Buzzer
34	PTPEH1213CCZZ	AB		C	Adhesive tape (for buzzer)
35	QCNTM1023CCZZ	AB		C	Contact
36	JKNBZ1225CC02	AA		C	Slide switch knob
37	LX-BZ1023ECZZ	AA		C	Screw
38	PTPEH1542CCZZ	AA		C	SHEET



2 PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	DUNT-1434ECZZ	AV	N	E	LCD unit	
2	PGUMS1027ECZZ	AB		B	Rubber connector	
3	PSHEZ1463CCZZ	AA		C	Wire fixing sheet	
4	QCNCW1306CC1B	AK		C	Connector (12pin)	
5	RC-CZD105ECZZ	AC		C	Capacitor (1μF)	[C6~10,13]
6	RC-CZ1021CCZZ	AB		C	Capacitor (0.1μF)	[C14~16,19,21]
7	RC-KZ1054CCZZ	AB		C	Capacitor (50WV 0.1μF)	[C18]
8	RCRSZ1002ECZZ	AF		B	Crystal (3.58MHZ)	[X1]
9	RH-DZ1001ECZZ	AD		B	Diode (1SR148)	[D4]
10	RTRNH1003ECZZ	AE	N	B	Converter transformer	
11	RVR-Z2400QCN1	AF		B	Variable resistor (20KΩ)	[VR]
12	VCCCTQ1HH101J	AA	N	C	Capacitor (50WV 100PF)	[C11,12]
13	VCCCTQ1HH151J	AA	N	C	Capacitor (50WV 150PF)	[C4]
14	VCCCTQ1HH200J	AA		C	Capacitor (50WV 20PF)	[C17]
15	VCEAGU1AW476M	AA		C	Capacitor (10WV 47μF)	[C20]
16	VCEAGU1AW477M	AC		C	Capacitor (10WV 470μF)	[C1]
17	VCEAGU1CW106M	AA		C	Capacitor (16WV 10μF)	[C2]
18	VCEAGU1HW335M	AA		C	Capacitor (50V 3.3μF)	[C3,24]
19	VCKYPU1HB272K	AA		C	Capacitor (50WV 2700pF)	[C5]
20	VCKYTQ1HB681K	AA	N	C	Capacitor (50WV 680PF)	[C22,23]
21	VHDDAN202K/-1	AB		B	Diode (DAN202K)	[D1,2,5]
22	VHEHZ9C1///-1	AB		B	Zener diode (HZ9C1)	[D3]
23	VHiD43257G12L	BB		B	IC (D43257G12L)	[IC5]
24	VHiHD61202/-1	AS		B	IC (HD61202)	[IC1]
25	VHiHD61203/-1	AX		B	IC (HD61203)	[IC2]
26	VHiLZ8413AM-1	AV	N	B	IC (LZ8413AM)	[IC3]
27	VHiMN1280P/-1	AE		B	IC (MN1280P)	
28	VHiLH5310PD-1	AT	N	B	IC(LH5310PD)	[IC4]
29	VRS-TP2BD000J	AA		C	Resistor (1/8W 0Ω ±5%)	[R18~20]
30	VRS-TP2BD103J	AA		C	Resistor (1/8W 10KΩ ±5%)	[R24]
31	VRS-TP2BD104J	AA		C	Resistor (1/8W 100KΩ ±5%)	[R11,13~17,23,26~28]
32	VRS-TP2BD105J	AA		C	Resistor (1/8W 1.0MΩ ±5%)	[R10]
33	VRS-TP2BD182G	AA	N	C	Resistor (1/8W 1.8KΩ ±2%)	[R21]
34	VRS-TP2BD183G	AA		C	Resistor (1/8W 18KΩ ±2%)	[R22]
35	VRS-TP2BD220J	AA		C	Resistor (1/8W 22Ω ±5%)	[R3]
36	VRS-TP2BD243J	AA		C	Resistor (1/8W 24KΩ ±5%)	[R7]
37	VRS-TP2BD392J	AA		C	Resistor (1/8W 3.9KΩ ±5%)	[R25]
38	VRS-TP2BD4R7J	AA		C	Resistor (1/8W 4.7Ω ±5%)	[R1]
39	VRS-TP2BD472J	AA		C	Resistor (1/8W 4.7KΩ ±5%)	[R29]
40	VRS-TP2BD473J	AA		C	Resistor (1/8W 47KΩ ±5%)	[R12]
41	VRS-TP2BD680J	AA		C	Resistor (1/8W 68Ω ±5%)	[R4]
42	VRS-TP2BD682J	AA		C	Resistor (1/8W 6.8KΩ ±5%)	[R2]
43	VRS-TP2BD822J	AA		C	Resistor (1/8W 8.2KΩ ±5%)	[R5,6,8,9]
44	VSDTA114YK/-1	AC		B	Transistor (DTA114YK)	[DT1]
45	VSDTC144EK/-1	AC		B	Transistor (DTC144EK)	[DT2]
46	VS2SA1036KQRC	AB		B	Transistor (2SA1036KQRC)	[Tr3]
47	VS2SC2412K/-1	AB		B	Transistor (2SC2412K)	[Tr1,2,4]
	(Unit)					
901	DUNTK1461ECZZ	BS	N	E	Main PWB unit	

3 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	TINSE1203ECZZ	AT	N	E	Instruction book(E)	(for U.S.A.)
	TINSF1205ECZZ	AT	N	D	Instruction book(F)	(for Canada)
	TINSG1206ECZZ	AT	N	D	Instruction book(G)	(for Germany)
	TINSE1204ECZZ	AT	N	D	Instruction book(E)	(for other countries)
2	SPAKC0496ECZZ	AE	N	D	Packing case	(for U.S.A.)
	SPAKC0499ECZZ	AE	N	D	Packing case	(for Canada)
	SPAKC0500ECZZ	AE	N	D	Packing case	(for other countries)
3	SPAKA0484ECZZ	AE	N	D	Packing cushion(tray)	
4	SSAKA0006UCZZ	AA		D	Vinyl bag (50×60)	
5	SSAKH0015HCZZ	AA		D	Vinyl bag (180×280)	
6	PHOG-1003ECZZ	AA	N	D	Protection paper	
	TLABM1290ECZZ	AC	N	D	Name plate label	(for U.S.A.)
	TLABM1287ECZZ	AB	N	D	Name plate label	(except for U.S.A.)